## CLAIMS

What is claimed is:

1. A descriptor system for transferring incoming data from a peripheral to a host and outgoing data from the host to the peripheral using a shared memory, the descriptor system comprising:

an outgoing data descriptor ring in the shared memory, the outgoing data descriptor ring storing outgoing data descriptors indicating locations of outgoing data buffers in the shared memory;

an incoming data descriptor ring in the shared memory, the incoming data descriptor ring storing incoming data descriptors indicating locations of incoming data buffers in the shared memory;

an incoming data status ring in the shared memory, the incoming data status ring storing incoming data status entries corresponding to incoming data in the incoming data buffers;

a control status block in the shared memory, the control status block comprising:

an outgoing data descriptor read pointer indicating a location of an outgoing data descriptor in the outgoing data descriptor ring, wherein the outgoing data descriptor read pointer indicates a number of outgoing data buffers to which the host can write outgoing data; and

an incoming data status pointer indicating a location of an incoming data status entry in the incoming data status ring, wherein the incoming data status pointer indicates a number of incoming data buffers from which the host can read incoming data; and

a descriptor management system in the peripheral, the descriptor management comprising:

an outgoing data descriptor write pointer indicating a location of an outgoing data descriptor in the outgoing data descriptor ring, wherein the outgoing data descriptor write pointer indicates a number of outgoing data buffers from which the peripheral can read outgoing data; and

an incoming data descriptor pointer indicating a location of an incoming data descriptor in the incoming data descriptor ring, wherein the incoming data descriptor pointer indicates a number of incoming data buffers to which the peripheral can write incoming data.

2. The system of claim 1, wherein the host is adapted to read a current outgoing data descriptor read pointer from the control status block, to write outgoing data to one or more outgoing data buffers according to the current outgoing data descriptor read pointer, to write one or more outgoing data descriptors to the outgoing data descriptor ring according to the current outgoing data descriptor read pointer, and to write an updated outgoing data descriptor write pointer to the descriptor management system in the peripheral according to the number of outgoing data buffers to which outgoing data was written, and wherein the peripheral is adapted to read one or more outgoing data descriptors from the outgoing data descriptor ring according to the updated outgoing data descriptor write pointer, to read outgoing data from one or more outgoing data buffers according to the one or more outgoing data descriptors, and to write an updated outgoing data descriptor read pointer to the control status block according to the number of outgoing data buffers from which the peripheral read outgoing data.

3. The system of claim 2, wherein the updated outgoing data descriptor write pointer comprises an address in the shared memory indicating a location in the outgoing data descriptor ring just beyond the most recent outgoing data descriptor written to the outgoing data descriptor ring by the host.

4. The system of claim 3, wherein the updated outgoing data descriptor read pointer comprises an address in the shared memory indicating a location in the outgoing data descriptor ring just beyond the most recent outgoing data descriptor read from the outgoing data descriptor ring by the peripheral.

5. The system of claim 2, wherein the updated outgoing data descriptor read pointer comprises an address in the shared memory indicating a location in the outgoing data descriptor ring just beyond the most recent outgoing data descriptor read from the outgoing data descriptor ring by the peripheral.

6. The system of claim 2, wherein the peripheral is adapted to read one or more incoming data descriptors from the incoming data descriptor ring according to a current incoming data descriptor pointer, to write incoming data to one or more incoming data buffers according to the one or more incoming data descriptors, to write one or more incoming data status entries in the incoming data status ring according to the one or more incoming data descriptors, and to write an updated incoming data status pointer to the control status block according to a number of incoming data buffers to which incoming data was written by the peripheral, and wherein the host is adapted to read the updated incoming data status pointer from the control status block, to read one or more incoming data status entries from the incoming data status ring according to the updated incoming data status pointer, to read incoming data from one or more incoming data buffers according to the updated incoming data status pointer, and to write an updated incoming data descriptor pointer to the descriptor management system in the peripheral according to the number of incoming data buffers from which the host read incoming data.

7. The system of claim 6, wherein the peripheral is adapted to write incoming data interrupt information to the control status block in the shared memory and to interrupt the host after writing the one or more incoming data status entries in the incoming data status ring, wherein the peripheral interrupts the host after writing the incoming data interrupt information to the control status block, and wherein the host is adapted to read the incoming data interrupt information from the control status block after being interrupted by the peripheral.

8. The system of claim 6, wherein the updated incoming data status pointer comprises an address in the shared memory indicating a location in the incoming data

status ring just beyond the most recent incoming data status entry written by the peripheral.

9. The system of claim 8, wherein the updated incoming data descriptor pointer comprises an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

10. The system of claim 6, wherein the updated incoming data descriptor pointer comprises an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

11. The system of claim 6, wherein the control status block is smaller than a cache line size for a cache memory associated with the host, and wherein the peripheral is adapted to update the entire contents of the control status block in the shared memory in a single write operation.

12. The system of claim 11, wherein each status ring entry is smaller than the cache line size for a cache memory associated with the host.

13. The system of claim 6, wherein each status ring entry is smaller than the cache line size for a cache memory associated with the host.

14. The system of claim 2, wherein the control status block is smaller than a cache line size for a cache memory associated with the host, and wherein the peripheral is adapted to update the entire contents of the control status block in the shared memory in a single write operation.

15. The system of claim 2, wherein each status ring entry is smaller than the cache line size for a cache memory associated with the host.

16. The system of claim 1, wherein the peripheral is adapted to read one or more incoming data descriptors from the incoming data descriptor ring according to a current incoming data descriptor pointer, to write incoming data to one or more incoming data buffers according to the one or more incoming data descriptors, to write one or more incoming data status entries in the incoming data status ring according to the one or more incoming data descriptors, and to write an updated incoming data status pointer to the control status block according to a number of incoming data buffers to which incoming data was written by the peripheral, and wherein the host is adapted to read the updated incoming data status pointer from the control status block, to read one or more incoming data status entries from the incoming data status ring according to the updated incoming data status pointer, to read incoming data from one or more incoming data buffers according to the updated incoming data status pointer, and to write an updated incoming data descriptor pointer to the descriptor management system in the peripheral according to the number of incoming data buffers from which the host read incoming data.

17. The system of claim 16, wherein the peripheral is adapted to write incoming data interrupt information to the control status block in the shared memory and to interrupt the host after writing the one or more incoming data status entries in the incoming data status ring, wherein the peripheral interrupts the host after writing the incoming data interrupt information to the control status block, and wherein the host is adapted to read the incoming data interrupt information from the control status block after being interrupted by the peripheral.

18. The system of claim 16, wherein the updated incoming data status pointer comprises an address in the shared memory indicating a location in the incoming data status ring just beyond the most recent incoming data status entry written by the peripheral.

19. The system of claim 18, wherein the updated incoming data descriptor pointer comprises an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

20. The system of claim 16, wherein the updated incoming data descriptor pointer comprises an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

21. The system of claim 1, wherein the control status block is smaller than a cache line size for a cache memory associated with the host, and wherein the peripheral is adapted to update the entire contents of the control status block in the shared memory in a single write operation.

22. The system of claim 1, wherein each status ring entry is smaller than the cache line size for a cache memory associated with the host.

23. A descriptor system for transferring incoming data from a peripheral to a host and outgoing data from the host to the peripheral using a shared memory, the descriptor system comprising:

a plurality of outgoing data descriptor rings in the shared memory, the outgoing data descriptor rings being individually associated with a corresponding outgoing data priority and storing outgoing data descriptors indicating locations of outgoing data buffers in the shared memory;

a plurality of incoming data descriptor rings in the shared memory, the incoming data descriptor rings being individually associated with a corresponding incoming data priority and storing incoming data descriptors indicating locations of incoming data buffers in the shared memory;

a plurality of incoming data status rings in the shared memory, the incoming data status rings being individually associated with a corresponding incoming data priority and storing incoming data status entries corresponding to incoming data in the incoming data buffers;

a control status block in the shared memory, the control status block comprising:

a plurality of outgoing data descriptor read pointers, the outgoing data descriptor read pointers being individually associated with a corresponding outgoing data priority and indicating a location of an outgoing data descriptor in a corresponding outgoing data descriptor ring, wherein the outgoing data descriptor read pointers individually indicate a number of outgoing data buffers to which the host can write outgoing data associated with the corresponding outgoing data priority; and

a plurality of incoming data status pointers, the incoming data status pointers being individually associated with a corresponding incoming data priority and indicating a location of an incoming data status entry in a corresponding incoming data status ring, wherein the incoming data status pointers individually indicate a number of incoming data buffers from which the host can read incoming data associated with the corresponding incoming data priority; and

a descriptor management system in the peripheral, the descriptor management comprising:

a plurality of outgoing data descriptor write pointers, the outgoing data descriptor write pointers being individually associated with a corresponding outgoing data priority and indicating a location of an outgoing data descriptor in a corresponding outgoing data descriptor ring, wherein the outgoing data descriptor write pointers individually indicate a number of outgoing data buffers from which the peripheral can read outgoing data associated with the corresponding outgoing data priority; and

a plurality of incoming data descriptor pointers, the incoming data descriptor pointers being individually associated with a corresponding incoming data priority and indicating a location of an incoming data descriptor in a

corresponding incoming data descriptor ring, wherein the incoming data descriptor pointers individually indicate a number of incoming data buffers to which the peripheral can write incoming data associated with the corresponding incoming data priority.

24. A descriptor system for transferring incoming data from a peripheral to a host using a shared memory, the descriptor system comprising:

an incoming data descriptor ring in the shared memory, the incoming data descriptor ring storing incoming data descriptors indicating locations of incoming data buffers in the shared memory;

an incoming data status ring in the shared memory, the incoming data status ring storing incoming data status entries corresponding to incoming data in the incoming data buffers;

a control status block in the shared memory, the control status block comprising an incoming data status pointer indicating a location of an incoming data status entry in the incoming data status ring, wherein the incoming data status pointer indicates a number of incoming data buffers from which the host can read incoming data; and

a descriptor management system in the peripheral, the descriptor management comprising an incoming data descriptor pointer indicating a location of an incoming data descriptor in the incoming data descriptor ring, wherein the incoming data descriptor pointer indicates a number of incoming data buffers to which the peripheral can write incoming data;

wherein the incoming data descriptors in the incoming data descriptor ring individually indicate the location of a plurality of incoming data buffers in the shared memory.

25. A method for transferring incoming data from a peripheral to a host and outgoing data from the host to the peripheral using a shared memory, the method comprising:

providing an outgoing data descriptor ring in the shared memory, the outgoing data descriptor ring storing outgoing data descriptors indicating locations of outgoing data buffers in the shared memory;

providing an incoming data descriptor ring in the shared memory, the incoming data descriptor ring storing incoming data descriptors indicating locations of incoming data buffers in the shared memory;

providing an incoming data status ring in the shared memory, the incoming data status ring storing incoming data status entries corresponding to incoming data in the incoming data buffers;

providing a control status block in the shared memory, the control status block comprising an outgoing data descriptor read pointer indicating a location of an outgoing data descriptor in the outgoing data descriptor ring, and an incoming data status pointer indicating a location of an incoming data status entry in the incoming data status ring;

providing a descriptor management system in the peripheral, the descriptor management comprising an outgoing data descriptor write pointer indicating a location of an outgoing data descriptor in the outgoing data descriptor ring, and an incoming data descriptor pointer indicating a location of an incoming data descriptor in the incoming data descriptor ring;

writing outgoing data to one or more outgoing data buffers in the shared memory using the host according to the outgoing data descriptor read pointer;

updating the outgoing data descriptor write pointer using the host to indicate a number of outgoing data buffers from which the peripheral can read outgoing data;

reading outgoing data from one or more outgoing data buffers in the shared memory using the peripheral according to the outgoing data descriptor write pointer;

updating the outgoing data descriptor read pointer using the peripheral to indicate a number of outgoing data buffers to which the host can write outgoing data;

writing incoming data to one or more incoming data buffers in the shared memory using the peripheral according to the incoming data descriptor pointer;

updating the incoming data status pointer using the peripheral to indicate a number of incoming data buffers from which the host can read incoming data;

reading incoming data from one or more incoming data buffers in the shared memory using the host according to the incoming data status pointer; and

updating the incoming data descriptor pointer using the host to indicate a number of incoming data buffers to which the peripheral can write incoming data.

26. The method of claim 25:

wherein writing outgoing data to one or more outgoing data buffers comprises the host reading a current outgoing data descriptor read pointer from the control status block, writing outgoing data to one or more outgoing data buffers according to the current outgoing data descriptor read pointer, and writing one or more outgoing data descriptors to the outgoing data descriptor ring according to the current outgoing data descriptor read pointer;

wherein updating the outgoing data descriptor write pointer comprises the host writing an updated outgoing data descriptor write pointer to the descriptor management system in the peripheral according to the number of outgoing data buffers to which outgoing data was written;

wherein reading outgoing data from one or more outgoing data buffers comprises the peripheral reading one or more outgoing data descriptors from the outgoing data descriptor ring according to the updated outgoing data descriptor write pointer and reading outgoing data from one or more outgoing data buffers according to the one or more outgoing data descriptors; and

wherein updating the outgoing data descriptor read pointer comprises the peripheral writing an updated outgoing data descriptor read pointer to the control status block according to the number of outgoing data buffers from which the peripheral read outgoing data.

27. The method of claim 26, wherein writing an updated outgoing data descriptor write pointer comprises the host writing to the outgoing data descriptor write pointer an address in the shared memory indicating a location in the outgoing data

descriptor ring just beyond the most recent outgoing data descriptor written to the outgoing data descriptor ring by the host.

28. The method of claim 27, wherein writing an updated outgoing data descriptor read pointer comprises the peripheral writing to the outgoing data descriptor read pointer an address in the shared memory indicating a location in the outgoing data descriptor ring just beyond the most recent outgoing data descriptor read from the outgoing data descriptor ring by the peripheral.

29. The method of claim 26, wherein writing an updated outgoing data descriptor read pointer comprises the peripheral writing to the outgoing data descriptor read pointer an address in the shared memory indicating a location in the outgoing data descriptor ring just beyond the most recent outgoing data descriptor read from the outgoing data descriptor ring by the peripheral.

30. The method of claim 26:

wherein writing incoming data to one or more incoming data buffers comprises the peripheral reading one or more incoming data descriptors from the incoming data descriptor ring according to a current incoming data descriptor pointer, writing incoming data to one or more incoming data buffers according to the one or more incoming data descriptors, and writing one or more incoming data status entries in the incoming data status ring according to the one or more incoming data descriptors;

wherein updating the incoming data status pointer comprises the peripheral writing an updated incoming data status pointer to the control status block according to a number of incoming data buffers to which incoming data was written by the peripheral;

wherein reading incoming data from one or more incoming data buffers comprises the host reading the updated incoming data status pointer from the control status block, reading one or more incoming data status entries from the incoming data status ring according to the updated incoming data status pointer, and reading incoming data from

one or more incoming data buffers according to the updated incoming data status pointer; and

wherein updating the incoming data descriptor pointer comprises the host writing an updated incoming data descriptor pointer to the descriptor management system in the peripheral according to the number of incoming data buffers from which the host read incoming data.

31. The method of claim 30, further comprising:

the peripheral writing incoming data interrupt information to the control status block in the shared memory;

the peripheral interrupting the host after writing the one or more incoming data status entries in the incoming data status ring and after writing the incoming data interrupt information to the control status block; and

the host reading the incoming data interrupt information from the control status block after being interrupted by the peripheral.

32. The method of claim 30, wherein writing an updated incoming data status pointer comprises the peripheral writing to the incoming data status pointer an address in the shared memory indicating a location in the incoming data status ring just beyond the most recent incoming data status entry written by the peripheral.

33. The method of claim 32, wherein writing an updated incoming data descriptor pointer comprises the host writing to the incoming data descriptor pointer an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

34. The method of claim 30, wherein writing an updated incoming data descriptor pointer comprises the host writing to the incoming data descriptor pointer an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

35. The method of claim 25, further comprising the peripheral updating the entire contents of the control status block in the shared memory in a single write operation.

36. The method of claim 25:

wherein writing incoming data to one or more incoming data buffers comprises the peripheral reading one or more incoming data descriptors from the incoming data descriptor ring according to a current incoming data descriptor pointer, writing incoming data to one or more incoming data buffers according to the one or more incoming data descriptors, and writing one or more incoming data status entries in the incoming data status ring according to the one or more incoming data descriptors;

wherein updating the incoming data status pointer comprises the peripheral writing an updated incoming data status pointer to the control status block according to a number of incoming data buffers to which incoming data was written by the peripheral;

wherein reading incoming data from one or more incoming data buffers comprises the host reading the updated incoming data status pointer from the control status block, reading one or more incoming data status entries from the incoming data status ring according to the updated incoming data status pointer, and reading incoming data from one or more incoming data buffers according to the updated incoming data status pointer; and

wherein updating the incoming data descriptor pointer comprises the host writing an updated incoming data descriptor pointer to the descriptor management system in the peripheral according to the number of incoming data buffers from which the host read incoming data.

37. The method of claim 36, further comprising:

the peripheral writing incoming data interrupt information to the control status block in the shared memory;

the peripheral interrupting the host after writing the one or more incoming data status entries in the incoming data status ring and after writing the incoming data interrupt information to the control status block; and

the host reading the incoming data interrupt information from the control status block after being interrupted by the peripheral.

38. The method of claim 36, wherein writing an updated incoming data status pointer comprises the peripheral writing to the incoming data status pointer an address in the shared memory indicating a location in the incoming data status ring just beyond the most recent incoming data status entry written by the peripheral.

39. The method of claim 38, wherein writing an updated incoming data descriptor pointer comprises the host writing to the incoming data descriptor pointer an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

40. The method of claim 36, wherein writing an updated incoming data descriptor pointer comprises the host writing to the incoming data descriptor pointer an address in the shared memory indicating a location in the incoming data descriptor ring just beyond the most recent incoming data descriptor written by the host.

41. The method of claim 25, further comprising:

the peripheral writing incoming data interrupt information to the control status block in the shared memory;

the peripheral interrupting the host after writing the one or more incoming data status entries in the incoming data status ring and after writing the incoming data interrupt information to the control status block; and

the host reading the incoming data interrupt information from the control status block after being interrupted by the peripheral.